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APPLICATION FOR UNITED STATES PATENT

FOR

PROCESS FOR FORMING A DIRECT BUILD-UP LAYER ON AN ENCAPSULATED DIE PACKAGE AND INTERMEDIATE STRUCTURES FORMED THEREWITH

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layer 206. However in such true CSP, the surface area provided by the microelectronic die active surface 204 generally does not provide enough surface for all of the external contacts needed to contact the external component (not shown) for certain types of microelectronic dice (e.g., logic).

5 Additional surface area can be provided through the use of an interposer, such as a substrate (substantially rigid material) or a flex component (substantially flexible material). FIG. 10 illustrates a substrate interposer 222 having a microelectronic die 224 attached to and in electrical contact with a first surface 226 of the substrate interposer 222 through small solder balls 228. The small solder balls 228 extend between contacts 10 232 on the microelectronic die 224 and conductive traces 234 on the substrate interposer first surface 226. The conductive traces 234 are in discrete electrical contact with bond pads 236 on a second surface 238 of the substrate interposer 222 through vias 242 that extend through the substrate interposer 222. External contacts 244 (shown as solder balls) are formed on the bond pads 236. The external contacts 244 are 15 utilized to achieve electrical communication between the microelectronic die 224 and an external electrical system (not shown).

The use of the substrate interposer 222 requires number of processing steps. These processing steps increase the cost of the package. Additionally, even the use of the small solder balls 228 presents crowding problems which can result in shorting 20 between the small solder balls 228 and can present difficulties in inserting underfilling between the microelectronic die 224 and the substrate interposer 222 to prevent contamination and provide mechanical stability.

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FIG. 11 illustrates a flex component interposer 252 wherein an active surface 254 of a microelectronic die 256 is attached to a first surface 258 of the flex component interposer 252 with a layer of adhesive 262. The microelectronic die 256 is encapsulated in an encapsulation material 264. Openings are formed in the flex component interposer 252 by laser ablation through the flex component interposer 252 to contacts 266 on the microelectronic die active surface 254 and to selected metal pads 268 residing within the flex component interposer 252. A conductive material layer is formed over a second surface 272 of the flex component interposer 252 and in the openings. The conductive material layer is patterned with standard photomask/etch processes to form conductive vias 274 and conductive traces 276. External contacts are formed on the conductive traces 276 (shown as solder balls 278 surrounded by a solder mask material 282 proximate the conductive traces 276).

The use of a flex component interposer 252 requires gluing material layers which form the flex component interposer 252 and requires gluing the flex component interposer 252 to the microelectronic die 256. These gluing processes are relatively difficult and may increase the cost of the package. Furthermore, the resulting packages have been found to have poor reliability.

Therefore, it would be advantageous to develop new apparatus and techniques to provide additional surface area to form traces for use in CSP applications, while utilizing commercially available, widely practiced semiconductor fabrication techniques.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIGS. 1a-1j are side cross-sectional views of a first embodiment of a process of forming a microelectronic package, according to the present invention;

FIG. 2 is a side cross-sectional view of an embodiment of a microelectronic assembly that includes a plurality of microelectronic dice, according to the present invention;

FIG. 3 is a side cross-sectional view of another embodiment of a microelectronic assembly that includes a plurality of microelectronic dice, according to the present invention;

FIG. 4 is a side cross-sectional view of still another embodiment of a microelectronic assembly that includes a plurality of microelectronic dice, according to the present invention;

FIG. 5 is a side cross-sectional view of yet another embodiment of a microelectronic assembly that includes a plurality of microelectronic dice, according to the present invention;

FIGS. 6a-6c are side cross-sectional views of a layering method for forming microelectronic packages, according to the present invention;

FIG. 7 is a top plan view of a patterned adhesive layer on a microelectronic assembly, according to the present invention;

FIG. 8 is a top plan view of an alternate patterned adhesive layer on a microelectronic assembly, according to the present invention;

FIG. 9 is a cross-sectional view of a true CSP of a microelectronic device, as known in the art;

5 FIG. 10 is a cross-sectional view of a CSP of a microelectronic device utilizing a substrate interposer, as known in the art; and

FIG. 11 is a cross-sectional view of a CSP of a microelectronic device utilizing a flex component interposer, as known in the art.

10 DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

Although FIGs. 1a-1j and 2-8 illustrate various views of the present invention, these figures are not meant to portray microelectronic assemblies in precise detail. Rather, these figures illustrate microelectronic assemblies in a manner to more clearly convey the concepts of the present invention. Additionally, elements common between
15 the figures retain the same numeric designation.

The present invention includes a packaging technology that fabricates build-up layers on an encapsulated microelectronic die that has expanded area larger than that of the microelectronic die. FIGs. 1a-1j illustrate a first embodiment of a process of forming a microelectronic package of the present invention. As shown in FIG. 1a, a
20 protective film 104 is abutted against an active surface 106 of a microelectronic die 102 to protect the microelectronic die active surface 106 from any contaminants. The microelectronic die active surface 106 has at least one contact 108 disposed thereon. The contacts 108 are in electrical contact with integrated circuitry (not shown) within

the microelectronic die 102. The protective film 104 is preferably a substantially flexible material, such as Kapton[®] polyimide film (E. I. du Pont de Nemours and Company, Wilmington, Delaware), but may be made of any appropriate material, including metallic films. The protective film 104 may have a weak, thermally stable adhesive, such as silicone, which attaches to the microelectronic die active surface 106. This adhesive-type film may be applied prior to placing the microelectronic die 102 in a mold or other such equipment used for the encapsulation process. The protective film 104 may also be a non-adhesive film, such as a ETFE (ethylene - tetrafluoroethylene) or Teflon[®] film, which is held on the microelectronic die active surface 106 by an inner surface of the mold or other such equipment during the encapsulation process.

The microelectronic die 102 is then encapsulated with an encapsulation material 112, such as plastics, resins, epoxies, and the like, as shown in FIG. 1b, that covers a back surface 114 and side(s) 116 of the microelectronic die 102. The encapsulation of the microelectronic die 102 may be achieved by any known process, including but not limited to transfer and compression molding, and dispensing. The encapsulation material 112 provides mechanical rigidity, protects the microelectronic die 102 from contaminants, and provides surface area for the build-up of trace layers.

After encapsulation, the protective film 104 is removed, as shown in FIG. 1c, to expose the microelectronic die active surface 106. As also shown in FIG. 1c, the encapsulation material 112 is preferably molded to form at least one surface 110 which is substantially planar to the microelectronic die active surface 106. The encapsulation material surface 110 and the microelectronic die active surface 106 constitute the active surface 120 of the encapsulated microelectronic die assembly, which will be utilized in

shown in FIG. 1f, at least one conductive trace extends adjacent the microelectronic die active surface 106 and adjacent said encapsulation material surface 110.

The plurality of conductive traces 124 may be formed by any known technique, including but not limited to semi-additive plating and photolithographic techniques. An exemplary semi-additive plating technique can involve depositing a seed layer, such as sputter-deposited or electroless-deposited metal on the first dielectric layer 118. A resist layer is then patterned on the seed layer, such as a titanium/copper alloy, followed by electrolytic plating of a layer of metal, such as copper, on the seed layer exposed by open areas in the patterned resist layer. The patterned resist layer is stripped and portions of the seed layer not having the layer of metal plated thereon is etched away. Other methods of forming the plurality of conductive traces 124 will be apparent to those skilled in the art.

As shown in FIG. 1g, a second dielectric layer 126 is disposed over the plurality of conductive traces 124 and the first dielectric layer 118. The formation of the second dielectric layer 126 may be achieved by any known process, including but not limited to film lamination, spin coating, roll coating and spray-on deposition.

As shown in FIG. 1h, a plurality of second vias 128 are then formed through the second dielectric layer 126. The plurality of second vias 128 may be formed any method known in the art, including but not limited to laser drilling and, if the second dielectric layer 126 is photoactive, forming the plurality of second vias 128 in the same manner that a photoresist mask is made in a photolithographic process, as known in the art.

If the plurality of conductive traces 124 is not capable of placing the plurality of second vias 128 in an appropriate position, then other portions of the conductive traces are formed in the plurality of second vias 128 and on the second dielectric layer 126, another dielectric layer formed thereon, and another plurality of vias is formed in the dielectric layer, such as described in FIG. 1f–1h. The layering of dielectric layers and the formation of conductive traces can be repeated until the vias are in an appropriate position. Thus, portions of a single conductive trace be formed from multiple portions thereof and can reside on different dielectric layers.

A second plurality of conductive traces 132 may be formed, wherein a portion of each of the second plurality of conductive traces 132 extends into at least one of said plurality of second vias 128. The second plurality of conductive traces 132 each include a landing pad 134 (an enlarged area on the traces demarcated by a dashed line 140), as shown in FIG. 1i.

Once the second plurality of conductive traces 132 and landing pads 134 are formed, they can be used in the formation of conductive interconnects, such as solder bumps, solder balls, pins, and the like, for communication with external components (not shown). For example, a solder mask material 136 can be disposed over the second dielectric layer 126 and the second plurality of conductive traces 132 and landing pads 134. A plurality of vias is then formed in the solder mask material 136 to expose at least a portion of each of the landing pads 134. A plurality of conductive bumps 138, such as solder bumps, can be formed, such as by screen printing solder paste followed by a reflow process or by known plating techniques, on the exposed portion of each of the landing pads 134, as shown in FIG 1j.

FIG. 2 illustrates another embodiment of the present invention wherein a plurality of microelectronic dice 102 are simultaneously encapsulated in the encapsulation material 112. The build-up layers of dielectric material and conductive element are simply represented as first build-up layer 152, second build-up layer 154, and third build-up layer 156 without illustrating the detail shown in FIGs. 1a-1j. It is, of course, understood that the microelectronic dice 102 could be encapsulated such that the microelectronic die back surfaces 114 are exposed, such that heat dissipation devices may be subsequently attached thereto, as shown in FIG. 3. Furthermore, as shown in FIG. 4, heat dissipation devices, such as heat slugs 158, could be thermally attached to the microelectronic die back surface 114, preferably with a thermally conductive adhesive (not shown), and encapsulated with the encapsulation material 112. Moreover, a microelectronic package core 150 could be utilized as a packaging material along with the encapsulation material 112 in the fabrication of the microelectronic package, such as illustrated in FIG. 5. The microelectronic package core 150 preferably comprises a substantially planar material. The material used to fabricate the microelectronic package core 150 may include, but is not limited to, a Bismaleimide Triazine ("BT") resin based material, an FR4 material (a flame retarding glass/epoxy material), and various polyimide materials. With the structures as shown in FIGs. 2-5, the individual microelectronic dice 102 are generally separated from one another in a singulation process (i.e., cutting through the encapsulation material 112 between the microelectronic dice 102 (FIGs. 2-4) or through the microelectronic package core 150 (FIG. 5)). Thus, the term "packaging material" is herein defined to include items such as the encapsulation material 112 and/or the microelectronic package core 150.

Although the build-up layer techniques described of FIGs. 1a-1j and 2-5 have many advantages, warpage induced by CTE (coefficient of thermal expansion) mismatch between the encapsulation material 112 and the dielectric layers (e.g., see dielectric layer 118 and 126 of FIGs. 1e-1i) used in the build-up layers can be significant. In general, the CTE of the dielectric layers is much larger than the CTE of the encapsulation material 112 (and microelectronic die 102). The dielectric layers are generally cured at elevated temperatures, which can result in the development of significant warpage when the assembly is cooled down. This warpage causes problems in subsequent processing steps. Thus, the following process has been developed to greatly reduce or substantially eliminate the warpage problem.

As shown in FIG. 6a, a first encapsulated die assembly 160 is provided. The first encapsulated die assembly 160 has a plurality of microelectronic dice 102 encapsulated in an encapsulation material 112 and a microelectronic package core 150 (similar to the structure shown in FIG. 5 without the build-up layers). As shown in FIG. 6b, a second encapsulated die assembly 162, which is similar to configuration of the first encapsulated die assembly 160, is attached to the first encapsulated die assembly 160.

As with the first encapsulated die assembly 160, the second encapsulated die assembly 162 also has a plurality of microelectronic dice 102' encapsulated in an encapsulation material 112'. The first encapsulated die assembly 160 and the second encapsulated die assembly 162 are oriented such that the first encapsulated microelectronic die assembly back surface 130 faces the second encapsulated microelectronic die back surface 130'.

The first encapsulated die assembly 160 and the second encapsulated die assembly 162 are preferably attached together with a layer of adhesive 164. In one

embodiment, the adhesive layer 164 comprises a weak, easily removable adhesive, such as silicone- or acrylic-based material. In another embodiment, the adhesive layer 164 comprises a sol-gel material that becomes porous and brittle after drying so that debonding is achieved by fracturing the sol-gel material. In a further embodiment, the adhesive layer 164 comprises a dissolvable adhesive, wherein the adhesive dissolves in an appropriate solvent (e.g., water, alcohol, etc.). When a dissolvable adhesive is used, the adhesive layer 164 can be patterned to allow a solvent to more easily flow between the first encapsulated die assembly 160 and the second encapsulated die assembly 162 to more quickly dissolve the adhesive layer 164. FIG. 7 illustrates such a patterned adhesive layer 164 on the first encapsulated die assembly 160.

It is, of course, understood that a strong adhesive could be used as the adhesive layer 164. As shown in FIG. 8, the strong adhesive layer 164 is patterned directly in a position where a dicing saw will cut the first encapsulated die assembly 160 and the second encapsulated die assembly 162 during a subsequent singulation process. Thus, the adhesive layer 164 is also removed during the singulation process.

Referring again to FIG. 6b, once the first encapsulated die assembly 160 and the second encapsulated die assembly 162 are adhered together, build-up layers can be formed on a first encapsulated microelectronic die assembly active surface 120 and on a second encapsulated microelectronic die assembly active surface 120', as shown in FIG. 6c. The build-up layers of dielectric material and conductive element are simply represented as first build-up layer 152, second build-up layer 154, and third build-up layer 156 on the first encapsulated die assembly 160 and as first build-up layer 152', second build-up layer 154', and third build-up layer 156' without illustrating the detail

shown in FIGs. 1a-1j. It is, of course, understood that the build-up layers can be formed simultaneously on the first encapsulated die assembly 160 and the second encapsulated die assembly 162.

Due to "back-to-back" attachment of the first encapsulated die assembly 160 and the second encapsulated die assembly 162, any tendency for warpage occurring in the first encapsulated die assembly 160 will be counteracted by a substantially equal but opposite tendency for warpage occurring in the second encapsulated die assembly 162, which greatly reduces or substantially eliminates the warpage problem. Furthermore, the ability to form the build-up layers (and potentially other process steps) simultaneously improves the efficiency of microelectronic die fabrication process.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.